## CLAIMS

We claim:

1. A method of fabricating final spacers each having a target width, comprising the steps of:

providing a structure having a gate electrode portion formed thereover; the gate electrode portion having a top and opposing side walls;

forming initial spacers over the opposing side walls of the gate electrode portion; the initial spacers each having an initial width that is less than the target width;

determining the difference between the initial width of the initial spacers and the target width;

forming a second spacer layer upon the initial spacers and the structure, the second spacer layer having a thickness that is equal to the determined difference between the initial width of the initial spacers and the target width; and

etching at least the second spacer layer from over the initial spacers and the structure to leave second spacer layer portions extending from the initial spacers to form the final spacers.

2. The method of claim 1, wherein the second spacer layer portions each having a width that is substantially equal to the thickness of the second spacer layer; the width of the second spacer layer portions plus the initial width of the initial spacers being equal to the target width.

3. The method of claim 1, wherein the structure is comprised of silicon.

4. The method of claim 1, wherein the structure is a silicon substrate.

5. The method of claim 1, wherein the gate electrode portion is comprised of polysilicon; the initial spacers are comprised of SiN; and the second spacer layer is comprised of SiN.

6. The method of claim 1, wherein the gate electrode portion has a thickness of from about 1000 to 3000Å; and the initial spacers each have a thickness of from about 250 to 350Å.

7. The method of claim 1, wherein the gate electrode portion has a thickness of from about 1700 to 2300Å; and the initial spacers each have a thickness of from about 280 to 320Å.

8. The method of claim 1, wherein the initial spacers each have a thickness of about 300Å.

9. The method of claim 1, including the step of forming a gate oxide layer between the structure and the gate electrode portion before the formation of the initial spacers.

10. The method of claim 1, wherein the initial spacers each include an overlying portion of oxide; and including the step of:

removing the overlying portions of oxide by an oxide wet dip process before the formation of the second spacer layer.

11. The method of claim 1, wherein the initial spacers each include an overlying portion of LPTEOS; and including the step of:

removing the overlying portions of LPTEOS by an oxide wet dip process before the formation of the second spacer layer.

12. The method of claim 1, including the step of forming silicide portions over the final spacers.

13. The method of claim 1, including the step of forming a composite oxide/nitride/oxide layer between the initial spacers and the opposing side walls of the gate electrode portion.

14. A method of fabricating final spacers each having a target width, comprising the steps of:

providing a structure having a gate electrode portion formed thereover; the gate electrode portion having a top and opposing side walls;

forming initial spacers over the opposing side walls of the gate electrode portion; the initial spacers each having an initial width that is less than the target width;

determining the difference between the initial width of the initial spacers and the target width;

forming a second spacer layer upon the initial spacers and the structure, the second spacer layer having a thickness that is equal to the determined difference between the initial width of the initial spacers and the target width; and

etching at least the second spacer layer from over the initial spacers and the structure to leave second spacer layer portions extending from the initial spacers to form the final spacers; wherein the second spacer layer portions each having a width that is substantially equal to the thickness of the second spacer layer; the width of the second spacer layer portions plus the initial width of the initial spacers being equal to the target width.

15. The method of claim 14, wherein the structure is comprised of silicon.

16. The method of claim 14, wherein the structure is a silicon substrate.

17. The method of claim 14, wherein the gate electrode portion has a thickness of from about 1000 to 3000Å; and the initial spacers each have a thickness of from about 250 to 350Å.

18. The method of claim 14, wherein the gate electrode portion has a thickness of from about 1700 to 2300Å; and the initial spacers each have a thickness of from about 280 to 320Å.

19. The method of claim 14, wherein the initial spacers each have a thickness of about 300Å.

20. The method of claim 14, including the step of forming a gate oxide layer between the structure and the gate electrode portion before the formation of the initial spacers.

21. The method of claim 14, including the step of forming a gate oxide layer between the structure and the gate electrode portion before the formation of the initial spacers; the gate oxide layer being comprised of LPTEOS, TEOS, PECVD or SACVD.

22. The method of claim 14, wherein the initial spacers each include an overlying portion of oxide; and including the step of:

removing the overlying portions of oxide by an oxide wet dip process before the formation of the second spacer layer.

23. The method of claim 14, wherein the initial spacers each include an overlying portion of LPTEOS; and including the step of:

removing the overlying portions of LPTEOS by an oxide wet dip process before the formation of the second spacer layer.

24. The method of claim 14, including the step of forming silicide portions over the final spacers.

25. The method of claim 14, including the step of forming a composite oxide/nitride/oxide layer between the initial spacers and the opposing side walls of the gate electrode portion.

26. A method of fabricating final spacers each having a target width, comprising the steps of:

providing a structure having a gate electrode portion formed thereover; the gate electrode portion having a top and opposing side walls; the gate electrode portion being comprised of polysilicon;

forming initial spacers over the opposing side walls of the gate electrode portion; the initial spacers each having an initial width that is less than the target width; the initial spacers being comprised of SiN;

determining the difference between the initial width of the initial spacers and the target width;

forming a second spacer layer upon the initial spacers and the structure, the second spacer layer having a thickness that is equal to the determined difference between the initial width of the initial spacers and the target width; the second spacer layer being comprised of SiN; and

etching at least the second spacer layer from over the initial spacers and the structure to leave second spacer layer portions extending from the initial spacers to form the final spacers; wherein the second spacer layer portions each having a width that is substantially equal to the thickness of the second spacer layer; the

width of the second spacer layer portions plus the initial width of the initial spacers being equal to the target width.

27. The method of claim 26, wherein the structure is comprised of silicon.

28. The method of claim 26, wherein the structure is a silicon substrate.

29. The method of claim 26, wherein the gate electrode portion is comprised of polysilicon; the initial spacers are comprised of SiN; and the second spacer layer is comprised of SiN.

30. The method of claim 26, wherein the gate electrode portion has a thickness of from about 1000 to 3000Å; and the initial spacers each have a thickness of from about 250 to 350Å.

31. The method of claim 26, wherein the gate electrode portion has a thickness of from about 1700 to 2300Å; and the initial spacers each have a thickness of from about 280 to 320Å.

32. The method of claim 26, wherein the initial spacers each have a thickness of about 300Å.

33. The method of claim 26, including the step of forming a gate oxide layer between the structure and the gate electrode portion before the formation of the initial spacers.

34. The method of claim 26, including the step of forming a gate oxide layer between the structure and the gate electrode portion before the formation of the initial spacers; the gate oxide layer being comprised of LPTEOS, TEOS, PECVD or SACVD.

35. The method of claim 26, including the step of forming a gate oxide layer between the structure and the gate electrode portion before the formation of the initial spacers; the gate oxide layer being comprised of LPTEOS.

36. The method of claim 26, wherein the initial spacers each include an overlying portion of oxide; and including the step of:

removing the overlying portions of oxide by an oxide wet dip process before the formation of the second spacer layer.

37. The method of claim 26, wherein the initial spacers each include an overlying portion of LPTEOS; and including the step of:

removing the overlying portions of LPTEOS by an oxide wet dip process before the formation of the second spacer layer.

38. The method of claim 26, including the step of forming silicide portions over the final spacers.

39. The method of claim 26, including the step of forming a composite oxide/nitride/oxide layer between the initial spacers and the opposing side walls of the gate electrode portion.